CMP–28/32

Reduce Spins – Improve SI Design Confidence – Identify Simple and Common Issues – Meet Schedules

FEATURES

- 3D-EM benchmark structures
- Material Extraction Method and Supporting Structures
- Resonators and Beatty Standard
- EDA Simulation-Measurement for each structure
- TDNA-VNA analysis structure
- TDR resolvers for ultra-fast TDR (10 psec and 28 psec rise times)
- Allegro layout available for easy 3D EM import

APPLICATIONS

- Benchmark Simulations, Test Meshing, Port Boundaries, Solver approach
- Improve Signal Integrity Methodology of Common Structures (voids, VIAS, etc.)
- 10-32 Gbpsec Simulation to Measurement of Jitter
- VNA, TDNA measurement validation to 50 GHZ, 8psec resolution

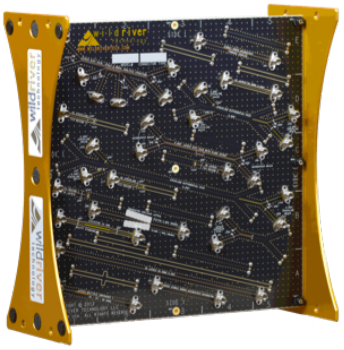
2015 BEST in Design & Test FINALIST

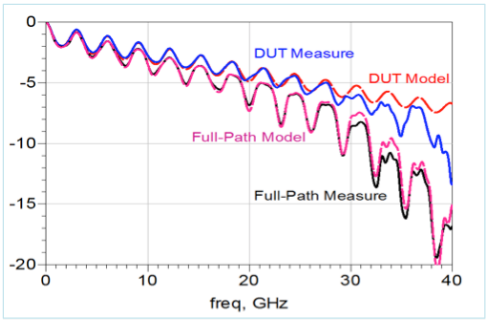
CMP–28/32 Channel Modeling EDA Package

Package Contents:

- **CMP-28 - 32 Gbpsec, CMP-32 - 50 Gbpsec**
- **S-parameters, pre-tested for quality**
- **PCB layout design files**
- **One library of your choice**
- **Keysight Technologies ADS**
- **Simbeor**
- **Mentor Hyperlynx-Nimbic**
- **Ansoft HFSS**

The **CMP-28** and **CMP-32** Channel Modeling Platforms represent a powerful tool for development of high-speed 50 GHz systems. optional low skew <1 psec matched cable kit. The primary target application for this product is 3D-EM solver analysis versus time and frequency domain measurement methodology. All structures include de-embedding to isolate the device-under-test (DUT) using Symmetrical De-embedding such as Automatic Fixture Removal (AFR, both 1X and 2X) or Measure-Modeled based.





EDA includes modeling of full path (includes VLF connector models) and de-embedded versions

wild river technology